Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-19 (Canceled)

Claim 20 (New): A serial access memory comprising:

a first memory array including a plurality of first memory cells, a first sense amplifier and a pair of first bit lines connected to the first memory cells and the first sense amplifier;

a second memory array including a plurality of second memory cells, a second sense amplifier and a pair of second bit lines connected to the second memory cells and the second sense amplifier;

a pair of column lines selectively connected to the first bit lines or the second bit lines, the column lines being located substantially parallel with the first and second bit lines;

a write register connected to the column lines;

a read register connected to the column lines;

a control circuit selectively connecting the column lines with the first bit lines or the second bit lines; and

an input/output circuit selectively connected to the registers.

Claim 21 (New): A serial access memory according to claim 20, wherein the input/output circuit includes an input circuit selectively connected to the write register and an output circuit selectively connected to the read register.

Claim 22 (New): A serial access memory according to claim 20, further comprising an additional read register connected to the column lines and an additional output circuit connected to the additional read register.

Claim 23 (New): A serial access memory according to claim 20, wherein the control circuit comprises:

a first transfer circuit connected between the column lines and the first bit lines, the first transfer circuit connecting the column lines with the first bit lines in response to a first control signal; and

a second transfer circuit connected between the column lines and the second bit lines, the second transfer circuit connecting the column lines with the second bit lines in response to a second control signal.

Claim 24 (New): A serial access memory according to claim 23, further comprising:

a third transfer circuit connected between the column lines and the read register,

the third transfer circuit connecting the column lines with the read registers in response to a third control signal; and

a fourth transfer circuit connected between the read register and the input/output circuit, the fourth transfer circuit connecting the read register with the input/output circuit in response to a fourth control signal.

Claim 25 (New): A serial access memory according to claim 24, further comprising:

a fifth transfer circuit connected between the column lines and the write register, the fifth transfer circuit connecting the column lines with the write register in response to a fifth control signal; and

a sixth transfer circuit connected between the write register and the input/output circuit, the sixth transfer circuit connecting the write register with the input/output circuit in response to a sixth control signal.

Claim 26 (New): A serial access memory according to claim 20, wherein the read register is selectively connected to two pairs of column lines, and the write register is selectively connected to the two pairs of column lines.

Claim 27 (New): A serial access memory comprising:

a first memory array including a plurality of first memory cells, a first sense amplifier and a pair of first bit lines connected to the first memory cells and the first

sense amplifier;

a second memory array including a plurality of second memory cells, a second sense amplifier and a pair of second bit lines connected to the second memory cells and the second sense amplifier;

a column line selectively connected to one of the first bit lines or one of the second bit lines, the column line being located substantially parallel with the first and second bit lines;

a register connected to the column line;

a control circuit selectively connecting the column line with the one of the first bit lines or the one of the second bit lines; and

an input/output circuit selectively connected to the register.

Claim 28 (New): A serial access memory according to claim 27, wherein the input/output circuit includes an input circuit and an output circuit, and the register includes a read register and a write register, and wherein the input circuit is selectively connected to the write register and the output circuit is selectively connected to the read register.

Claim 29 (New): A serial access memory according to claim 28, further comprising an additional read register connected to the column line and an additional output circuit connected to the additional read register.

Claim 30 (New): A serial access memory according to claim 27, wherein the control circuit comprises:

a first transfer circuit connected between the column line and the one of the first bit lines, the first transfer circuit connecting the column line with the one of the first bit lines in response to a first control signal; and

a second transfer circuit connected between the column line and the one of the second bit lines, the second transfer circuit connecting the column line with the one of the second bit lines in response to a second control signal.

Claim 31 (New): A serial access memory according to claim 30, further comprising a third transfer circuit connected between the column line and the register, the third transfer circuit connecting the column line with the register in response to a third control signal.

Claim 32 (New): A serial access memory according to claim 27, wherein the register is selectively connected to two column lines.

Claim 33 (New): A serial access memory comprising:

a first memory array including a plurality of first memory cells, a plurality of first sense amplifiers and a plurality of pairs of first bit lines each of which is connected to

the first memory cells and the first sense amplifiers;

a second memory array including a plurality of second memory cells, a plurality of second sense amplifiers and a plurality of pairs of second bit lines each of which is connected to the second memory cells and the second sense amplifiers;

a plurality of column lines selectively connected to one of the first bit lines or one of the second bit lines, the column lines being located substantially parallel with the first and second bit lines;

a plurality of registers each of which is connected to one of the column lines;

a control circuit selectively connecting one of the column lines with one of the first bit lines or the second bit lines; and

a plurality of input/output circuits each of which is selectively connected to one of the registers.

Claim 34 (New): A serial access memory according to claim 33, wherein the input/output circuits include a plurality of input circuits and a plurality of output circuits, and the registers include a plurality of read registers and a plurality of write registers, and wherein the input circuits are selectively connected to the write registers and the output circuits are selectively connected to the read registers.

Claim 35 (New): A serial access memory according to claim 34, further comprising a plurality of additional read registers connected to the column lines and a plurality of

additional output circuits connected to the additional read registers.

Claim 36 (New): A serial access memory according to claim 33, wherein the control circuit comprises:

a first transfer circuit connected between the column lines and the first bit lines, the first transfer circuit connecting the column lines with the first bit lines in response to a first control signal; and

a second transfer circuit connected between the column lines and the second bit lines, the second transfer circuit connecting the column lines with the second bit lines in response to a second control signal.

Claim 37 (New): A serial access memory according to claim 36, further comprising a third transfer circuit connected between the column lines and the register, the third transfer circuit connecting the column lines with the registers in response to a third control signal.

Claim 38 (New): A serial access memory according to claim 33, wherein one of the registers is selectively connected to two of the column lines.